MS APPEAL BRIEF - PATENTS
Docket No.: 0630-1524P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Sung-il PARK et al.

Application No.: 09/550,282 Confirmation No.: 9574

Filed: April 14, 2000 Art Unit: 2871

For: LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE Examiner: Z. Q. Qi

APPEAL BRIEF TRANSMITTAL FORM

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief on behalf of the Appellants in connection with the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

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A Notice of Appeal was filed on January 23, 2006.

☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27.

The fee has been calculated as shown below:

☐ Extension of time fee pursuant to 37 C.F.R. §§ 1.17 and 1.136(a) - $@@@.

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Dated: March 23, 2006

Respectfully submitted,

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
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Sir:

Appellants hereby appeal from the decision in the final Office Action dated September 22, 2005 finally rejecting claims 1, 3-6, 11-15, 17 and 19-26. As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case January 3, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal for this Application is LG. Philips LCD Co., Ltd., as evidenced by an Assignment recorded on October 26, 2000 at Reel 011348, Frame 0757.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

To the best of Appellants' knowledge, there are no other prior or pending appeals of this application, or patent interference proceedings, or judicial proceedings which may be related to, directly affect, or be directly affected by, or have a bearing on the Board's decision of this appeal.

III. STATUS OF CLAIMS

In the Application on appeal, claims 1, 3-6, 11-15, 17, and 19-26 are pending. Claims 1, 15 and 22 are independent. Claims 1, 3-6, 11-15, 17, and 19-26 are rejected and are on appeal.

IV. STATUS OF AMENDMENTS

The Amendment under 37 CFR 1.111, filed on August 18, 2005, has been entered. The status of the claims is correctly stated in that Amendment.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1 is directed to a liquid crystal display (LCD), comprising (1) a gate line, e.g., 100, formed on a transparent substrate, e.g., 1'; (2) a data line, e.g., 200, crossing said gate line and formed on said transparent substrate; (3) an insulating layer, e.g., 220, electrically insulating said data line from said gate line; (4) a thin film transistor formed at an intersection of said gate line and said data line, and connected to said gate line and said data line, the thin film transistor being disposed in an area having a channel area, a source area, e.g., 160, and a drain area, e.g., 180; (5) a passivation layer, e.g., 240, formed over the thin film transistor; (6) a pixel electrode, e.g., 300 and/or 300' or 300", having portions thereof formed on the surface of the passivation layer, but not over the thin film transistor; (7) a low reflective layer, e.g., 230, covering at least a portion of at least one of said gate line and said data line and covering the area to shield the light passing the gate line, the data line and the area; and (8) an upper substrate located above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding layer, see, for example, Fig. 8.

B. Claim 15 is directed to a method of manufacturing a liquid crystal display, comprising (1) forming a gate line and a gate electrode of a thin film transistor to be connected with the gate line on a transparent substrate; (2) forming an insulating layer electrically insulating said gate line and the gate electrode; (3) forming a data line and source electrode and drain electrode over said transparent substrate the source electrode and the drain electrode being respectively disposed in a source area and a drain area, at least one electrode of the source electrode and the drain electrode being connected with the data line; (4) forming a passivation layer over the thin film transistor; (5) forming a pixel electrode with portions thereof on the surface of the passivation layer, but not over the thin film transistor; (6) first forming a low reflective layer over at least a portion of at least one of said gate line and said data line and on the channel region, the source area and the drain area; and (7) forming an upper substrate above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding layer - see Figs. 5-8 which illustrate partially complete devices and a substantially complete device made based on the claimed method.

C. Claim 22 is directed to a method of manufacturing a liquid crystal display, comprising (1) forming a gate line and gate electrode connected thereto on a transparent substrate; (2) forming an insulating layer over said gate line and gate electrode; (3) forming a semiconductor layer over said gate electrode; (4) forming a data line crossing said gate line, a source electrode connected to said data line and on a first portion of said semiconductor layer, and a drain electrode on a second portion of said semiconductor layer; (5) forming a low reflective layer over at least a portion of at least one of said gate line and said data line and on the first and second portions; (6) forming a passivation layer having a contact hole exposing said drain electrode over said transparent substrate; (7) forming a pixel electrode with portions thereof disposed on said passivation layer but not over the thin film transistor, and connected to said drain electrode via said contact hole; and (8) forming an upper substrate above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding - see Figs. 5-8 which illustrate partially complete devices and a substantially complete device made based on the claimed method.

VI. GROUNDS OF OBJECTION AND REJECTION TO BE REVIEWED ON APPEAL

A. Claim 15 is objected to for reciting "...forming a gate line and a gate electrode of a thin film transistor to be connected with the gate line on a transparent substrate; forming an insulating layer electrically insulating said gate line and the gate electrode..."

B. Claims 1, 11, 14-15, 22 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,259,200 to Morita et al. (hereinafter, "Morita").

C. Claims 3, 4, 17, 19 and 26 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita, as applied above, and further in view of U.S. Patent 6,172,728 to Hiraishi and U.S. Patent 6,172,723 to Inoue et al. ("Inoue").

D. Claims 12, 13, 23 and 24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi.

E. Claims 5, 6, 20 and 21 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi, and further in view of "Appellants' admitted prior art (AAPA)".

VII. ARGUMENT

A. Claim 15 is objected to for reciting "...forming a gate line and a gate electrode of a thin film transistor to be connected with the gate line on a transparent substrate; forming an insulating layer electrically insulating said gate line and the gate electrode..." The final Office Action states that this claim should recite an insulating layer electrically insulating the gate line and the gate electrode from the data line.

Appellants respectfully disagree.

The final Office Action explains why the gate electrode is not insulated from the gate line. Appellants agree with the analysis. However, the language in issue, which is also found in claim 22 and is not objected to in claim 22, does not state forming an insulating layer electrically insulating the gate line from the gate electrode. The language in issue merely recites forming an insulating layer separating both the gate electrode and the gate line. It does not state what those elements are insulated from, nor does it have to.

As pointed out in the Amendment filed on March 14, 2005, and in the Reply filed on August 18, 2005, this language is found in originally filed claim 22, so there is proper basis for the language as part of Appellants' originally filed disclosure, nor does this final Office Action find fault with the identical language in claim 22.

Appellants also respectfully submit that they are entitled to claim what they regard as their invention, especially, as here, where open-ended claim terminology is used.

Reconsideration and reversal of this objection are respectfully requested.

B. Claims 1, 11, 14-15, 22 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,259,200 to Morita et al. (hereinafter, "Morita"). This rejection is respectfully traversed.

Complete discussions of the rejections are set forth in the final Office Action and are not being repeated here.

Independent claims 1, 15 and 22 recite a combination of features regarding a liquid crystal display (LCD) including (1) a pixel electrode having portions thereof formed on the surface of the passivation layer but not over the thin film transistor; and an upper substrate located above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black matrix or light shielding layer, or (2) a method of making the structure set forth in (1).

Appellants respectfully submit that this combination of features as set forth in independent claims 1, 15 and 22 is not disclosed or made obvious by the prior art of record.

Morita only discloses a low reflective layer 10x on its source line 10 "to preclude unwanted light reflection" (col. 4, lines 51-67). Morita does not disclose a low reflective metal layer disposed on one of the gate line and data line and the area having a channel area, a source area and a drain area, as recited. Moreover, Morita's upper substrate above the pixel electrode does disclose a black mask 62 that is a black layer and/or a light shielding layer, which is the opposite of what is recited in all of the claims.

Thus, Morita does not disclose or suggest the claimed invention.

The final Office Action asserts that Morita discloses certain features, but not other features.

In this regard, the final Office Action states that "there is no black matrix between the upper substrate (60) and the pixel electrode (14) in the Fig. 2..." Appellants respond by pointing out that Fig. 2 shows only part of the LCD. Figs. 4-6 disclose just the opposite, i.e., where the black mask 62 is directly above part of pixel electrode 14, and note that Morita is directed to "improve the aperture ratio of pixel" (col. 2, lines 6-7) and does this, in part, by providing an improved "black mask 62 [is] patterned in stripes on the opposing substrate. The black mask shields the gate lines 43, auxiliary lines 44 and this film transistors 3." Thus, a black mask that is

located between the substrate and the pixel electrode is an essential part of Morita's invention, contrary to the quoted statement in the final Office Action.

Thus, the rejection is fatally flawed for at least this reason, which is not addressed by the Examiner in any Office Action despite the fact that it was raised in a number of Appellants' papers.

The final Office Action concludes that it would be obvious to arrange the low reflective layer 10x on the data line or the gate line and on the channel area, source area, drain area, and to do away with the black matrix (actually, just a black layer 62) "for precluding light reflection."

Appellants respectfully disagree.

The Examiner has the initial duty of supplying the factual basis for the rejection he advances. An Examiner may not, because of doubts that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis. See, In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968).

Moreover, in making a rejection under 35 U.S.C. §103, the prior art as a whole must be considered. The teachings of the applied references are to be viewed as they would have been viewed by one of ordinary skill in the art. Kimberly-Clark v. Johnson & Johnson, 745 F.2d 1437, 1454, 223 USPQ 603, 614 (Fed. Cir. 1984); In re Mercier, 515 F.2d 1161, 1165, 185 USPQ 774, 778 (CCPA 1975). "It is impermissible within the framework of §103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In re Wesslau, 353 F.2d at 241, 147, USPQ at 393. In re Hedges, et al., 228 USPQ 685 (Fed. Cir. 1986).

If it were so obvious to modify Morita to remove any black layer from the upper substrate and to provide a low reflectivity layer on the gate electrode and drain electrode as well as on the data line, then why didn't Morita do it?

The final Office Action fails to offer any explanation of why Morita did not make the claimed invention. Appellants respectfully submit that it would not be obvious to modify Morita so drastically as suggested because it would not have been obvious to do so.

One reason it would not be obvious to modify Morita as suggested is because Morita teaches that the invention is "preferably provided with at least a shading black mask aligned with the gate line" and that the Morita device "needs to shade the row gate lines" (col. 2, 34-44).

These are positive teachings in the very same reference that provides the top layer of its signal lines 10 with low reflectivity layers 10x. Appellants respectfully submit that such positive teachings teach away from removing the black shade layer for the gate lines.

Moreover, because there is no teaching at all in Morita of using low reflectivity layers on the transistor electrodes, per se, and because Morita is well aware that such layers are provided on signal lines, and because there is no disclosed problem with Morita's transistor electrodes, or with its gate lines and drain lines, Appellants respectfully submit that one of ordinary skill in the art would have no incentive to go to the trouble and expense of providing such low reflectivity coatings on all these electrodes and lines.

Appellants respectfully submit that the only basis for modifying Morita as suggested is based solely on improper hindsight reconstruction of Appellants' invention based solely on Appellants' disclosure. Accordingly, the final Office Action does not provide proper motivation to one of ordinary skill in the art to apply a low-reflective film to the recited gate and drain line and transistor electrode areas of Morita. Nor does the final Office Action provide proper motivation for one of ordinary skill in the art to modify Morita by removing Morita's black shading layer that is explicitly taught as being needed, being an essential part of Morita's "improved" black mask, disclosed throughout the patent to improve over the shortcomings of prior art black masks.

Further to the arguments set forth above, Appellants make reference to the two full paragraphs in col. 6 of Morita that discuss the improved black mask of Morita's invention (see col. 1, lines 62-63 which discusses the need for an improved black mask). Morita's improved black mask 62 shields the gate line 43, auxiliary lines 44, thin film transistors 3, and auxiliary

capacitances Cs, while Morita's light-shielding film (shielding back light) is used as a black mask to prevent light passing through between the signal lines 10 and the pixel electrodes 14 and covers the domains where the liquid crystal orientation is disturbed at the edge portions of the pixel electrode 14.

In other words, a black mask is very much an essential part of Morita's invention.

On the other hand, Morita only devotes two sentences to the low reflectance layer on signal lines 10. All that Morita states, in the main body of its specification is "According to the present invention, the top insulating substrate 60 is provided with no black mask aligned with the signal lines 10. The top layer of the signal lines 10 of Al will cause its reflectance to be large enough to degrade the quality of image. For this reason, a top layer of a material (Cr, for example) having a relatively low reflectance is further applied on the Al film to preclude unwanted light reflection."

Instead of taking these two sentences in context, the final Office Action takes them out of context and speculates that it would be obvious to fundamentally change the "improved" black mask of Morita by eliminating it altogether and substituting a low reflectance layer on everything covered by Morita's black mask.

The exact rationale on which this rejection is based is found in the first full paragraph on page 5 of the final Office Action, which states that (1) Morita applies a relatively low reflective layer on the Al film to preclude unwanted light reflection; (2) and the low reflective layer shields the light to pass the signal line instead of the black matrix, and concludes, based on those two premises that it would be obvious to using the low reflective layer to cover the gate line, the source area, drain area and channel region instead of using a black matrix to shield the light passing the gate line and channel area, source area and drain area so as to preclude unwanted light reflection.

Appellants respectfully submit that the second premise on which this conclusion is drawn is invalid for the following reasons, and that the conclusion of obviousness itself is invalid at least because it is based on an invalid premise, as well as for other reasons discussed herein.

Morita's display only removes the black mask strips on the upper substrate that are aligned with the signals lines and the edge portion of the pixel electrodes, and does this by aligning light shielding film strips underneath the signal lines and pixel electrode edges, while retaining shading black mask strips aligned over the gate lines. The stated reason for retaining the shading black mask strips or lines aligned with the gate lines is to prevent light from passing around the gate lines and the thin film transistors (col. 2, lines 34-40). In other words, Morita prevents light from passing around its signal lines by arranging a light shielding film strips 5 underneath its signal lines 10, and prevents light from passing around its gate lines and thin film transistors by using shading black mask strips on the upper substrate, oriented perpendicular to the light shielding films 5 that are provided under the signal lines and pixel electrode edges - see col. 2, lines 7-65, and col. 4, lines 21-67 of Morita.

Morita's use of a relatively low reflectivity metal film on its signal lines is simply not used to solve the same problem that its upper substrate black mask strips and its lower substrate light shielding films are directed to address. As noted above, Morita's upper substrate black mask strips and its lower substrate light shielding films are used to prevent light from passing around the gate lines and the signal lines and the transistors and, because of this, they overlap those lines and the transistors (see col. 1, lines 46-63). Appellants respectfully submit that, in this way, the thin from transistors are shielded from stray light and light leakage between pixels is reduced.

Morita's use of a relatively low reflectivity coating on the signals lines is accomplished not to prevent light from passing around the gate lines and the signal lines and the transistors, but merely to reduce degradation of the image from unwanted light reflection (col. 4, last sentence). Morita most certainly does not explicitly, or inherently (i.e., necessarily), disclose that the relatively low reflection coatings reduce scattered light, or reduce light from passing around the gate lines, or reduce light from passing around the transistors, or reduce light from passing around the signal lines. Morita's relatively low reflectivity coatings are only used to reduce reflectivity that will reduce image quality, e.g., light reflected into a user's eyes that would reduce image contrast, where there is no black mask aligned with the signal lines.

The final Office Action provides absolutely no objective factual evidence that Morita includes explicit or inherent teachings that replacing the its parallel upper substrate shadow black matrix with low reflective coatings on the gate lines and the transistors would provide the same beneficial effects as Morita's shadow mask. As evidence of this, Morita only uses the low reflectivity coatings on the signal lines that also have light shields 5 that are explicitly taught to reduce stray light and backlight (col. 4, lines 34-39).

Appellants also respectfully submit that another reason to conclude that the low reflection electrode films 10x would not work as suggested in the final Office Action is that, if they worked so well, then Morita would not need to provide its light shielding films beneath the signal lines and pixel electrode edges, and could do away with his entire light shielding film invention as summarized in cols. 2-3, and discussed more in detail in col 4, which just does not make sense, and is another reason why the logic used as the basis for this rejection is flawed.

Moreover, Appellants respectfully submit that the proposed modification of Morita in view of Morita's own disclosure amounts to nothing more than an open an invitation to try such a speculative modification that Morita clearly did not try or disclose trying. Obviousness requires one of ordinary skill in the art have a reasonable expectation of success as to the invention "obvious to try" and "absolute predictability" is incorrect standards. In re O'Farrell, 853 F.2d 894, 903 [7 USPQ2d 1673] (Fed. Cir. 1988). The presence of a reasonable expectation of success is measured from the perspective of a person of ordinary skill in the art at the time the invention was made. Life Techs., Inc. v. Clontech Labs., Inc., 224 F.3d 1320, 1326 [56 USPQ2d 1186] (Fed.Cir. 2000).

In other words, there is nothing in Morita that would motivate one of ordinary skill in the art to drastically redesign Morita to eliminate Morita's improved black mask and substitute a low reflectance coating without any disclosure that such a drastic modification will have a reasonable expectation of producing an improved device. In fact, as discussed above, no such improvement would be expected.

In Appellants' view, the only possible suggestion for combining the applied prior art in the manner proposed by the Examiner to meet the above-noted claim features stems from hindsight knowledge derived from the Appellants' own disclosure. The use of such hindsight

knowledge to support an obviousness rejection under 35 U.S.C. §103 is, of course, impermissible. See, for example, W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir, 1983), cert. denied, 469 U.S. 851 (1984).

Because of these shortcomings of the rejection, the rejection fails to make out a prima facie case of proper motivation to modify Morita and, therefore, means that the final Office Action fails to make out a prima facie case of obviousness of the claimed invention because a showing of a suggestion, teaching, or motivation to combine the prior art references is an "essential evidentiary component of an obviousness holding." C.R. Bard, Inc. v. M3 Sys. Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998).

Thus, the final Office Action fails to make out a prima facie case of obviousness of the invention recited in claims 1, 11, 14, 15, 22 and 25 and this rejection of claims 1, 11, 14, 15, 22 and 25 should be reversed.

C. Claims 3, 4, 17, 19 and 26 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita, as applied above, and further in view of U.S. Patent 6,172,728 to Hiraishi and U.S. Patent 6,172,723 to Inoue et al. ("Inoue").

Initially, Appellants respectfully submit that Morita does not make out a prima facie case of unpatentability of the claimed invention recited in the claims from which claims 3, 4, 17, 19 and 26 depend, i.e., claim 11 or claim 22, and neither Hiraishi nor Inoue are applied to remedy the aforementioned deficiencies of Morita.

Accordingly, this rejection is improper and should be reversed.

Moreover, Hiraishi provides gaps or notches in the gate lines and/or source lines to reduce areas where they overlap with the pixel electrodes and to reduce the parasitic capacitance of the device (col. 5, lines 45-65).

Appellants respectfully submit that one of ordinary skill in the art would not be motivated to modify Morita to overlap the pixel electrode with a gate line or data line based on Hiraishi when Hiraishi teaches minimizing such overlap and because such overlap will increase the

parasitic capacitance of the device, which Morita teaches away from doing - see col. 7, lines 28-54, for example.

Furthermore, Morita discloses a backlit LCD device (see Figs. 2 and 3, for example) that does not indicate that it needs its display quality increased, whereas Hiraishi discloses a reflective LCD device that needs to have its display quality enhanced by using a low reflective film on its gate lines and source lines. The final Office Action has not demonstrated that one of ordinary skill in the art would look to a reflective LCD display to modify a backlit display, especially where there is no indication of a need to improve the characteristics of the backlit LCD device.

Appellants note that although this argument, which was presented in the March 14, 2005 Amendment and in the Reply filed on August 18, 2005, was not addressed, per se, in any Office Action, the last two Office Actions state, in the "Response to Arguments" section dealing with the Morita reference, that "Morita discloses an active-matrix display that is not limited to use back light." Appellants respectfully disagree and note, in this regard, that the only disclosed embodiments of Morita operate using back light - see, for example, Figs. 1A, 2, 3 and 9A of Morita, which expressly disclose back light, and col. Col. 4, lines 34-39, which explicitly discloses that the light shielding films 5 are used to block a back light.

Moreover, the final Office Action admits that Hiraishi does not disclose placing a low reflectance coating on source or drain electrodes. The final Office Action merely states that it would be obvious to provide such a feature in Morita as "at least an obvious variation" because "forming a low reflectance layer on the gate electrode and on the source/drain electrode would be the same principle and would have the same function." Appellants respectfully disagree. The "same principle and same function" arguments may apply to the doctrine of equivalence for patent infringement analysis, but the issue involved here is proper motivation to modify primary reference that does not have this feature in view of a secondary reference that also does not have this feature, and this analysis simply does not fit.

Moreover, the speculation that it would be obvious to form a low reflectance layer on the gate electrode and on the source/drain electrode because it would involve the same principle and would have the same function is an improper "per se" rule of unpatentability. In other words, the

final Office Action improperly relies on the per se rule form a low reflectance layer on the gate electrode and on the source/drain electrode because it would involve the same principle and would have the same function as forming it on signal lines.

The final Office Action's position in this regard is completely at odds with established precedential case law of the Court of Appeals for the Federal Circuit. As stated by the Federal Circuit in In re Ochiai, 71 F.3d 1565, 1572, 37 USPQ2d 1127, 1133 (Fed. Cir. 1995), "reliance on per se rules of obviousness is legally incorrect and must cease."

During patent examination the PTO bears the initial burden of presenting a prima facie case of unpatentability. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444(Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788(Fed. Cir. 1984). This burden can be satisfied when the PTO presents evidence, by means of some teaching, suggestion or inference either in the applied prior art or generally available knowledge, that would have appeared to have suggested the claimed subject matter to a person of ordinary skill in the art or would have motivated a person of ordinary skill in the art to combine the applied references in the proposed manner to arrive at the claimed invention. See Carella v. Starlight Archery Pro Line Co., 804 F.2d 135, 140, 231 USPQ 644, 647 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); In re Rinehart, 531 F.2d 1048, 1051-1052, 189 USPQ 143, 147 (CCPA 1976).

If the PTO fails to meet this burden, then the Appellant is entitled to the patent. However, when a prima facie case is made, the burden shifts to the Appellant to come forward with evidence and/or argument supporting patentability. Patentability *vel non* is then determined on the entirety of the record, by a preponderance of evidence and weight of argument, In re Ochiai, cited above.

The Office may not shift this burden by making up its own improper "per se" rules of unpatentability, as it appears to have done here.

Furthermore, one of ordinary skill in the art would have no incentive to modify Morita in view of Hiraishi, as suggested, because Morita's transistor electrodes are all shielded by the

Morita's "improved" black mask and do not need the features provides by the low reflectance material. Additionally, the final Office Action fails to address the additional masking and etching steps that may be needed to provide such a suggested feature, steps that may well give a disincentive to provide such a feature.

The Office then turns to Inoue as evidence "that lights are mixed with light reflected from the reflection electrode and this mixed light lowers the image display quality." Inoue allegedly solves such a problem by patterning a low-reflection conductive film on a high conductive reflection film - col. 11, lines 34-50. The final Office Action continues by stating that gate electrodes, source electrodes and drain electrodes are electrical conductive films and would benefit from a low reflective film to enhance image quality.

Appellants respectfully disagree with this speculative reasoning for a number of reasons.

Firstly, none of the three applied references, including Inoue, disclose providing a low reflection film on any of the transistor electrodes, so there is no objective factual evidence that any of the three references provide any motivation to do so.

Secondly, the only objective factual evidentiary basis for an incentive to provide a low reflective layer on the gate electrode, source electrode and/or drain electrode is found in Appellants' disclosure, which may not be properly used against Appellants.

Thirdly, as pointed out above, one of ordinary skill in the art would have no incentive to modify Morita in view of Hiraishi, as suggested, because Morita's transistor electrodes are all shielded by the Morita's "improved" black mask and do not need the features provides by the low reflectance material. Additionally, the final Office Action fails to address the additional masking and etching steps that may be needed to provide such a suggested feature, steps that may well give a disincentive to provide such a feature.

Fourthly, Hiraishi's invention deals with reflective LCDs, not back-lit LCDs and the final Office Action has not shown that a teaching applicable to a reflective LCD will provide proper motivation to modify a back-lit LCD absent comparative data to show that the same conditions will exist in both devices. However, instead of providing objective factual evidence of this type,

the final Office Action merely provides speculation, which is not a proper basis for a rejection based on 35 U.S.C. §103(a).

Fifthly, Inoue discloses a reflection type liquid crystal device with a microlens array and focuses the light incident on the microlens array on highly reflective pixel regions, while providing a low reflectivity region surrounding the high reflectivity region to limit reflection of stray light passed by the microlens array (col. 2, lines 15-32). The problem faced by Inoue is not the problem facing Morita's backlit LCD device, which does not have a microlens array focusing light on highly reflective pixel areas, and does not depend on reflected light for its main mode of operation. The final Office Action has not provided objective factual evidence that one of ordinary skill in the art would look to Inoue to modify Morita alone, or Morita modified by Hirashi.

Accordingly, the final Office Action fails to make out a prima facie case of obviousness of the invention recited in claims 3, 4, 17, 19 and 26 and, this rejection should be reversed.

D. Claims 12, 13, 23 and 24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi. This rejection is respectfully traversed.

Initially, Appellants respectfully submit that Morita does not make out a prima facie case of unpatentability of the claimed invention recited in the claims from which claims 12, 13, 23 and 24 depend, i.e., claim 11 or claim 22, and Hiraishi is not applied to remedy the aforementioned deficiencies of Morita.

Accordingly, this rejection is improper and should be reversed.

Moreover, Morita, the base reference in the applied reference combination, does not disclose overlap of its pixel electrodes 14 with its gate lines 43 or with its data (signal) lines 10, and Hiraishi discloses reducing such overlap to reduce parasitic capacitance - see col. 5, lines 45-54. In view of this explicit teaching in Hiraishi, there would be no incentive to modify Morita to provide overlap between pixel electrodes and either (or both) data lines or gate lines. In fact, there would be an explicit disincentive to make the proposed modification of Morita. Thus, Hiraishi actually teaches away from being combined with Morita, as suggested.

A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the Appellant. The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the Appellant. See W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1550-51, 220 USPQ 303, 311 (Fed. Cir. 1983) (the totality of a reference's teachings must be considered), cert. denied, 469 U.S. 851 (1984); In re Sponnoble, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969) (references taken in combination teach away since they would produce a "seemingly inoperative device"); In re Caldwell, 319 F.2d 254, 256, 138 USPQ 243, 245 (CCPA 1963) (reference teaches away if it leaves the impression that the product would not have the property sought by the Appellant). See, In re Gurley, 31 USPQ2d 1130 (Fed. Cir. 1994).

Accordingly, the final Office Action fails to make out a prima facie case of proper motivation to modify Morita as suggested and therefore fails to make out a prima facie case of obviousness of the claimed invention.

Reconsideration and reversal of this rejection of claims 12, 13, 23 and 24 under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi is respectfully requested.

E. Claims 5, 6, 20 and 21 stand rejected under 35 U.S.C. §103(a) as unpatentable over Morita in view of Hiraishi, and further in view of "Appellants' admitted prior art (AAPA)".

This rejection is improper at least for the reasons that claim 1, from which claims 5, 6, 9 and 10 depend, and claim 15, from which claims 20 and 21 depend, are traversed, above. Additionally, Appellants have not made a clear, unequivocal and unmistakable admission of any prior art, including the "related art" disclosed in Figs. 1-4. The final Office Action has not presented any objective factual evidence to support a conclusion that Appellants have made a clear, unmistakable and unequivocal admission that Figs. 1-4 are prior art to Appellants. In order for something to be considered admitted prior art, the admission must be clear, unmistakable and unequivocal. See, in this regard, Fleming v. Giesa (BdPatApp&Int) 13 USPQ2d 1052 (7/17/1989); Harner et al. v. Barron et al., 215 USPQ 743 (Comr Pats 1981), Suh v. Hoefle

(BdPatApp&Int) 23 USPQ2d 1321 (4/30/1991); Issidorides v. Ley (BdPatApp&Int) 4 USPQ2d 1854 (4/2/1985); and Ex parte The Successor In Interest Of Robert S. McGaughey (BdPatApp&Int) 6 USPQ2d 1334 (3/4/1988).

Moreover, the fact that CrOx has a reflectivity of about 3% and may be widely used does not remedy the aforenoted deficiencies of the applied reference combination.

Accordingly, reconsideration and reversal of this rejection of claims 5, 6, 20 and 21 are respectfully requested.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: March 23, 2006

Respectfully submitted,

By Esther H. Chong

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/550,282:

1. (Previously Presented) A liquid crystal display (LCD), comprising:

a gate line formed on a transparent substrate;

a data line crossing said gate line and formed on said transparent substrate;

an insulating layer electrically insulating said data line from said gate line;

a thin film transistor formed at an intersection of said gate line and said data line, and connected to said gate line and said data line, the thin film transistor being disposed in an area having a channel area, a source area and a drain area;

a passivation layer formed over the thin film transistor;

a pixel electrode having portions thereof formed on the surface of the passivation layer, but not over the thin film transistor;

a low reflective layer for covering at least a portion of at least one of said gate line and said data line and covering the area to shield the light passing the gate line, the data line and the area; and

an upper substrate located above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding layer.

2. (Canceled)

3. (Previously Presented) The LCD of claim 26, wherein said low reflective layer is formed on said gate electrode.

4. (Previously Presented) The LCD of claim 26, wherein said thin film transistor includes a source electrode and a drain electrode; and

said low reflective layer is formed on said source and drain electrodes.

5. (Previously Presented) The LCD of claim 1, wherein said low reflective layer has a light reflectivity of 3% or less.

6. (Previously Presented) The LCD of claim 1, wherein said low reflective layer is formed of CrOx.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Previously Presented) The LCD of claim 1, wherein said passivation layer formed over said gate line, said data line, said low reflective layer and said pixel electrode formed on said passivation layer is connected via a contact hole in said passivation layer to said thin film transistor.

12. (Original) The LCD of claim 11, wherein said pixel electrode is formed over a portion of said data line.

13. (Original) The LCD of claim 11, wherein said pixel electrode is formed over a portion of said gate line.

14. (Original) The LCD of claim 11, further comprising:

a color filter substrate with color filters formed thereon; and

liquid crystal sealed between said color filter substrate and said transparent substrate.

15. (Previously Presented) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and a gate electrode of a thin film transistor to be connected with the gate line on a transparent substrate;

forming an insulating layer electrically insulating said gate line and the gate electrode;

forming a data line and source electrode and drain electrode over said transparent substrate the source electrode and the drain electrode being respectively disposed in a source area and a drain area, at least one electrode of the source electrode and the drain electrode being connected with the data line;

forming a passivation layer over the thin film transistor;

forming a pixel electrode with portions thereof on the surface of the passivation layer, but not over the thin film transistor;

first forming a low reflective layer over at least a portion of at least one of said gate line and said data line and on the channel region, the source area and the drain area;

forming an upper substrate above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding layer.

16. (Canceled)

17. (Previously Presented) The method of claim 15, wherein the step of first forming the low reflective layer includes the step of forming a low reflective layer covering said gate electrode.

18. (Canceled)

19. (Previously Presented) The method of claim 15, wherein said low reflective layer is formed covering said source electrode.

20. (Original) The method of claim 15, wherein said low reflective layer has a light reflectivity of 3% or less.

21. (Original) The method of claim 15, wherein said low reflective layer is formed of CrOx.

22. (Previously Presented) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and gate electrode connected thereto on a transparent substrate;

forming an insulating layer over said gate line and gate electrode;

forming a semiconductor layer over said gate electrode;

forming a data line crossing said gate line, a source electrode connected to said data line and on a first portion of said semiconductor layer, and a drain electrode on a second portion of said semiconductor layer;

forming a low reflective layer over at least a portion of at least one of said gate line and said data line and on the first and second portions;

forming a passivation layer having a contact hole exposing said drain electrode over said transparent substrate;

forming a pixel electrode with portions thereof disposed on said passivation layer but not over the thin film transistor, and connected to said drain electrode via said contact hole; and

forming an upper substrate above the pixel electrode, wherein an area between said pixel electrode and said upper substrate, and above said low reflective layer, is free of any black layer or light shielding.

23. (Original) The method of claim 22, wherein said forming a pixel electrode step forms said pixel electrode to overlap a portion of said data line.

24. (Original) The method of claim 22, wherein said forming a pixel electrode step forms said pixel electrode to overlap a portion of said gate line.

25. (Previously Presented) The method of claim 22, further comprising:

forming a color filter on a color filter substrate; and

sealing the liquid crystal between said color filter substrate and said transparent substrate.

26. (Previously Presented) The LCD of claim 1, wherein the thin film transistor further includes:

a gate electrode connected to said gate line, said gate electrode being covered with the channel region; and

a source electrode, and a drain electrode connected to a drain line, the source electrode and the drain electrode being respectively covered with the low reflective layer.

PTO/SB/17 (12-04v2)
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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/550,282-Conf. #9574
Filing Date	April 14, 2000
First Named Inventor	Sung-il PARK
Examiner Name	Z. Q. Qi
Art Unit	2871
Attorney Docket No.	0630-1524P

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 02-2448 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- =	_____	x _____	=	_____

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- =	_____	x _____	=	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/50	_____	(round up to a whole number) x	_____	=	_____

4. OTHER FEE(S) Fees Paid ($)

Non-English Specification, $130 fee (no small entity discount)

Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal 500.00

SUBMITTED BY					
Signature	Esther H. Chong	Registration No. (Attorney/Agent)	40,953	Telephone	(703) 205-8000
Name (Print/Type)	Esther H. Chong			Date	March 23, 2006

EHC/RJW/vd